Remarks

Reconsideration of the above referenced application in view of the enclosed amendment and remarks is requested. Claims 31-38 have been added. Claims 1-3, 11-13, and 21-23 have been amended. Claims 1 to 38 are now pending in the application. A request for drawing corrections is submitted herein, to address Examiner's objection to Figure 3B. Figure 4 is also replaced to correct a reference numeral error. The Figures are described correctly in the Specification as originally filed, so as such, they do not introduce any new matter.

ARGUMENT

Claims 7, 8, 17, 18, 27 and 28 are rejected under 35 U.S.C. § 112, second paragraph. This rejection is moot based on the foregoing amendments and following discussion. Claims 1, 11 and 21 have been amended to reference a third device, thereby nullifying the Examiner's rejection based on antecedent basis.

Claims 1, 4-7, 9-11, 14-17, 19-21, 24-27 and 29-30 are rejected under 35 U.S.C. 102(b) as being unpatentable over Abraham et al. (US 5,237,616) (hereafter, Abraham et al.). This rejection is respectfully traversed and Claims 1, 4-7, 9-11, 14-17, 19-21, 24-27 and 29-30 are believed allowable as amended based on the foregoing and following discussion.

The Examiner references Figure 1 of Abraham et al. as showing the elements of Applicant's claimed invention. Abraham et al. teach a system for selectively connecting a processor 103 to either privileged memory 105 or unprivileged memory 109 via an application specific Integrated circuit (AISC [sic]) 107. Abraham does not show selectively switching a communication path of a third device to one of the host or first device, as claimed by Applicant. Abraham et al. clearly show a customized device (ASIC) performing the switch between two memories, where the host is connected to either the privileged or unprivileged memory.

In Claims 1, 11 and 21, Applicants recite an event which <u>selectively switches a communication path from a third device to one of said host and said first device</u>. At no time does Abraham et al. teach or suggest that communication path can be switched from a memory to a device <u>other than the host (processor)</u>. Thus, the claimed elements of Claims 1, 4-7, 9-11, 14-

17, 19-21, 24-27 and 29-30 are not taught or suggested by the cited references. Thus, Claims 1, 4-7, 9-11, 14-17, 19-21, 24-27 and 29-30 are allowable as amended.

With regard specifically to Claim 5, the Examiner asserts that the ASIC 107 shown in Figure 1 is equivalent to Applicant's recited first device comprising a logic device. This assertion is erroneous. The claimed logic device (first device) is connected to the host via a tap line. Abraham et al. teach that their logic device 107 is connected to the processor via a data/address bus 115. The connectivity of these two elements is different. Also, Applicant's claimed invention requires that an event selectively switches a communication path from a third device to one of said host and said first device. Abraham et al. teach a logic device that is always connected to both privileged memory and unprivileged memory. Abraham et al. also teach that data in both privileged memory and unprivileged memory can be read in both privileged mode using protected address space and unprivileged mode using unprotected address space but they can only be written in privileged mode. (Col. 2, lines 13-16) This contradicts a selective switching between devices, as recited in Applicant's claims.

Claims 1-3, 11-13 and 21-23 are rejected under 35 U.S.C. 102(b) as being unpatentable over Nozuyama (US 5,862,359) (hereafter, Nozuyama). This rejection is respectfully traversed and Claims 1-3, 11-13 and 21-23 are believed allowable as amended based on the foregoing and following discussions.

The Examiner asserts that Figure 1 of Nozuyama shows all of the elements of Applicant's claimed invention. The teachings of Nozuyama cannot be determined merely by looking at Figure 1 in a vacuum. Nozuyama teaches a data transfer bus including divisional buses connectable by bus switch circuit. A decoder 4 is required to control the bus switch 3 for connecting bus divisions. The Examiner asserts that functional block 14 combined with bus switch 3 show Applicant's first device. Further, the Examiner cites Col. 2, lines 20-25 as describing the tap line as recited in Applicant's claimed invention. These assertions are erroneous.

Applicant's claimed invention requires a first device initiating an event based on information received via a tap line, and wherein said event selectively switches a communication path from a third device to one of said host and said first device. The required tap line communicatively connecting a host with the first device is not shown by Nozuyama. Further, the

functional block and bus switch combined cannot be used as Applicant's first device and result in the claimed invention. If a communication path is formed using Nozuyama's bus divisions to communicatively connect functional block 14 and bus switch 3 (as a first device) and functional block 15, then there is no longer a communicative connection between the CPU (functional block 11) and the first device, i.e., the tap line. If functional block 14 and bus switch 3 are construed to be Applicant's first device, then Nozuyama's invention cannot operate as a selective communication path between either the host and third device or the first device and third device where the selection is ordered by the host and controlled by the first device. Nozuyama teaches only one divided signal line, a bus division line, as shown in Figure 1 (21,22,23). Nozuyama teaches that the CPU communicates directly with the bus switch. However, if the bus switch is to be combined with functional block 14 as the first device, the communication path between the CPU (host) and the first device may be severed if the communication path is selectively switched to the third device and first device. This is contrary to how Applicant's invention operates. Thus, the cited references do not teach or suggest the elements claimed by Applicant and Claims 1-3, 11-13 and 21-23 are allowable as amended.

Claims 8, 18, and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Abraham et al. This rejection is respectfully traversed and Claims 8, 18 and 28 are believed allowable as amended based on the foregoing and following discussion.

Abraham et al. shows that switching is controlled by an application specific integrated circuit (ASIC) 107. Applicant's claimed invention requires a field programmable gate array (FPGA). These elements have distinct features and are not the same type of element. Appendix A is an excerpt from a web page entitled "FPGA/ASIC Selection," and can be found on the Internet at

http://www.micro-circuit.com/index.cfm?PID=21&action1=displaylong&DocID=374.

This excerpt clearly shows that engineers must choose between the two types of integrated circuits (ASIC or FPGA) and that they are not equivalent. A FPGA is reprogrammable and an ASIC is custom programmed and unchangeable. Thus, the cited references do not show the recited elements of the claims and Claims 8, 18, and 28 are believed allowable as amended.

CONCLUSION

In view of the foregoing, claims 1-38 are all in condition for allowance. If the Examiner has any questions, the Examiner is invited to contact the undersigned at (703) 633-6845. Early issuance of Notice of Allowance is respectfully requested. Please charge any shortage of fees in connection with the filing of this paper, including extension of time fees, to Deposit Account 02-2666 and please credit any excess fees to such account.

Respectfully submitted,

Dated: 6-11-04

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Appendix A – Excerpt from Web Page entitled, "FPGA/ASIC Selection"

...technology applied

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FPGA/ASIC Selection

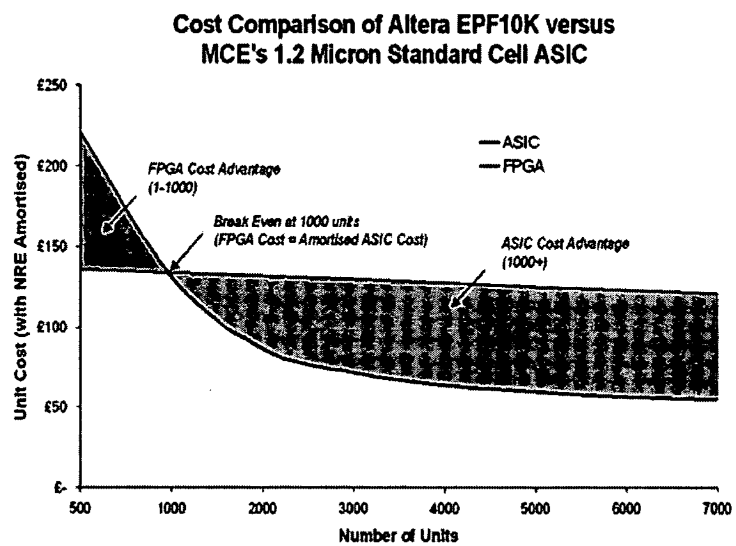
In the electrical design process, engineers are often faced with the selection of the most appropriate Integrated Circuit (IC) technology for their application. Although, for the majority of applications, the choice is made from standard "off the shelf" components, there are instances where special integrated circuits are required for a specific purpose. In this case, the debate often centres on the selection of components such as Field Programmable Gate Arrays (FPGAs) or Application Specific Integrated Circuits (ASICs). The selection process is normally a complex mixture of technical and economic factors and, ultimately, the choice may depend on the subjective opinion of the engineer rather than a full assessment of the options. For example, in digital applications, the electronic engineer may prefer a FPGA during the prototyping phase for the flexibility of programming and immediate availability of components. However, once the functionality has been demonstrated and the component needs to be utilised in production, a FPGA may well be unattractive from a cost point of view. ASICs offer the advantage of highly optimised logic and dedicated metal interconnect. As such they can match or better the functionality and performance of most FPGAs, with significant attendant cost reduction. The FPGA design data can be used in the conversion to an ASIC and, depending on the volumes required, semi -custom or full custom ASICs can be recommended.

Achieving a unit cost reduction is not the only reason MCE's customers wish to convert from FPGAs to ASICs; the other major driver is obsolescence in older FPGAs.

The table below compares and contrasts the primary features for selection of FPGAs and ASICs.

FPGAs	ASICs
• Suitable for low volumes • Flexibility in programming • Reduced non recurring engineering (NRE) costs • Short timescales for development • Digital applications only • Higher power consumption	• Suitable for medium and higher volumes • Fixed design • Non recurring engineering costs for tools and masks • Longer timescales • Digital, mixed signal and linear designs • Lower power consumption and reduced heat dissipation

For the unit costs, there is a single point at which the financial attractiveness of FPGAs and ASICs cross over. This is illustrated in the graph, which depicts a real example (Altera EPF10K50R versus MCE 1.2 μ m standard cell ASIC). In this example, the cross over point, taking the NRE conversion cost into account, occurs at 1000 units.



The crossover point for a particular application will depend on several factors including:

- Gate count requirement
- Speed
- RAM and Macros
- Pad count
- Package type
- Operating environment

These factors mainly determine the geometry, process and die size, which leads to the selection of the most appropriate semiconductor technology for the application.

MCE has many years experience of designing with ASICs and FPGAs and can offer an assessment of whether ASICs or FPGAs may be the most cost effective in the design of integrated circuits at all stages of the production cycle (i.e. concept design, prototyping, low, medium and high volume production). Sometimes, a hybrid approach using, for example, customised FPGAs, may be the most attractive technical and economic solution for particular applications.

Whether the best route is FPGA to ASIC, ASIC to customised FPGA or FPGA to customised FPGA, MCE can help.

For further information, please contact Sales or fill out on-line enquiry form.

Related documents, events, files

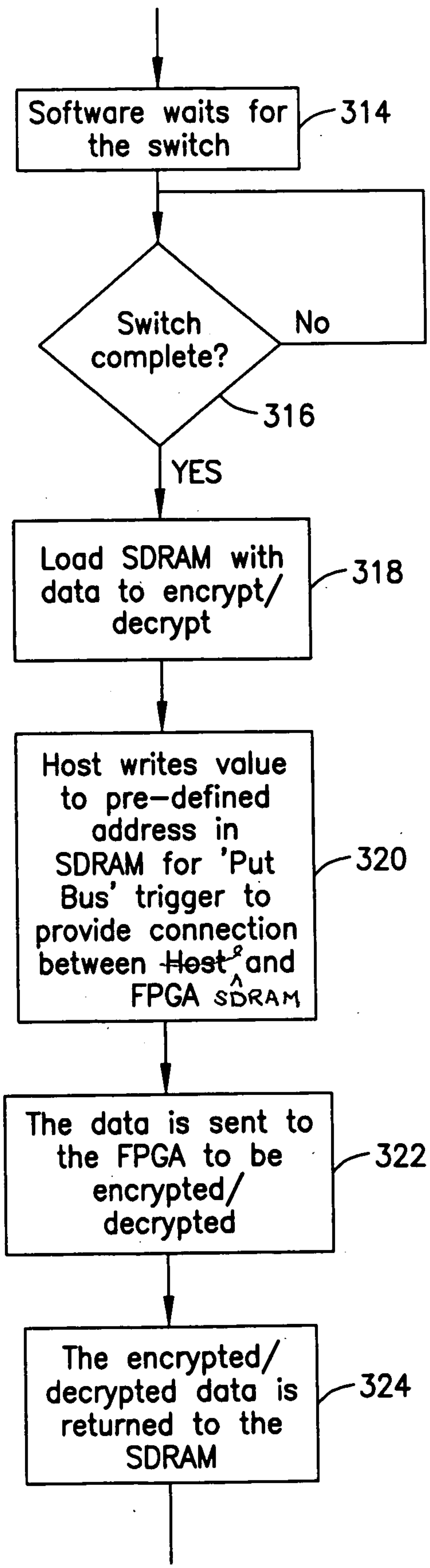
None

Author: Steve Riches
Last Update: Thursday,14 November 2002

Keywords used:

back

Fig. 3b


Software waits for the switch
314
Switch complete?
No
316
YES
Load SDRAM with data to encrypt/ decrypt
318
Host writes value to pre-defined address in SDRAM for 'Put Bus' trigger to provide connection between ~~Host~~ SDRAM and FPGA
320
The data is sent to the FPGA to be encrypted/ decrypted
322
The encrypted/ decrypted data is returned to the SDRAM
324

ANNOTATED MARKED-UP DRAWINGS
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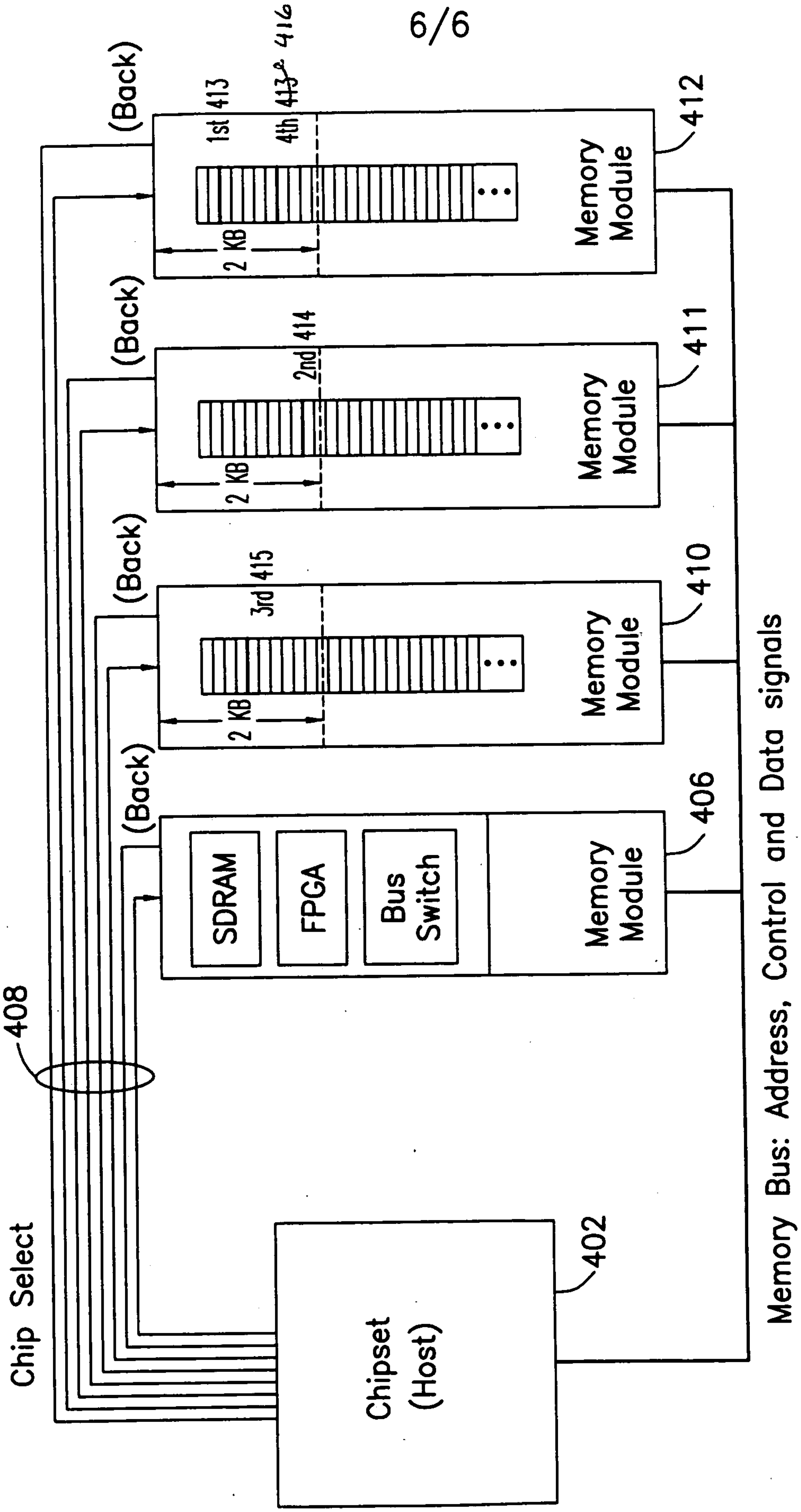

Fig. 4